REMARKS

This Amendment is filed in response to the final Office Action dated August 12, 2003, which has a shortened statutory period set to expire November 12, 2003.

Applicants thank the Examiner for the opportunity to participate in a telephone interview on September 10, 2003. During this telephone interview, Jeanette Harms (attorney for Applicants) discussed the distinctions between ROM and non-ROM (e.g. RAM, CAM, etc.). The Examiner requested that these distinctions be submitted in written format for his consideration. Although no resolution was reached in the telephone interview, the Examiner indicated that the ROM/non-ROM distinction was not found explicitly in the prior art and could be potentially patentable. A discussion of the distinctions between ROM/non-ROM now follows.

The Specification, at page 14, line 23 to page 15, line 10, teaches:

> It is appreciated that the test library 12 and the test library re-coding process 15 of the prior art (Figure 1) are eliminated in the IC design flow 300 of the present invention. Most cells of the simulation library 301, including ROMs, can be automatically converted into ATPG memory models 320 by the ATPG memory model generation process 310 of the present invention. Only complicated memories, such as RAMs and CAMs, may need be simplified before the ATPG memory model generation process 310 can automatically convert them into ATPG memory models 320. It should also be appreciated that the equivalence verification process 14 (Figure 1) is also eliminated. In the present invention, behavioral descriptions of ROMS contained in simulation library 301 are used directly by ATPG memory model generation process 310, whereas the simplified behavioral descriptions 340 of the RAM and CAMs can be verified against the simulation models contained within the simulation library 301 by using a commercially available behavioral simulator (e.g., a Verilog simulator) 305.

The Specification further teaches on page 16, lines 13-17:

> According to the present invention, ROMs generally do not need to be re-described because the behavioral descriptions for ROMs are generally not complex. Thus, ATPG memory model generation process 310 can directly read behavioral descriptions (or, behavioral models) from simulation library 301 and then build an internal model based on ATPG memory primitives 325.

The Specification further teaches on page 17, lines 15-24:

> Simulation models of RAMs are very complex, often having thousands of lines of behavioral Verilog that are organized based on the timing and layout of the RAM. In most cases, it is very difficult to extract a unit-delay or zero-delay functional model from the behavioral description of a RAM. Accordingly, in the present invention, behavioral descriptions of complicated memories are simplified by re-describing the memories with a predefined subset of behavioral Verilog. The simplified behavioral descriptions (or behavioral models) can then be automatically converted into ATPG memory models by process 310 in accordance with the present invention.

The Specification further teaches on page 31, line 23 to page 32, line 5, as follows:

> Content-addressable memories (CAMs) are common in high-performance designs. However, existing ATPG tools provide no or only clumsy features to model CAMs. As with RAMs, a CAM model should be flexible enough to model most CAMs in a simple manner, yet the ATPG model built must be very efficient. Yet, CAM modeling is even more challenging than RAM modeling because of the inherent complexity and variety of CAM designs. In the present embodiment, CAMs are modeled in a similar fashion the RAMs are modeled. CAM models, however, include a CPORT primitive for matching data from a data bus primitive to the content of a memory primitive.

Based on the above passages, which are representative and not limiting, Applicants respectfully submit that ROMs and non-

ROMs pose significantly different challenges in constructing a structural model for use in an ATPG.

Claims 1, 13, and 25 recite a limitation regarding this distinction. Claims 2-12 depend from Claim 1, Claims 14-24 depend from Claim 13, and Claims 26-36 depend from Claim 25.

Of importance, the distinction between ROMs and non-ROMs is not disclosed or suggested in the cited references. Neither Routine Expedient nor Official Notice can remedy that deficiency. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claims 1-36.

CONCLUSION

Claims 1-36 are pending in the present Application. Applicants respectfully request allowance of these claims.

If the next action in this case is other than allowance, please telephone the undersigned at 408-451-5907.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 12, 2003.

9/12/03
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